REMARKS

Status of the Claims

Claims 1-4, 7-19, 21-25 and 28 are pending.

Claims 1-4, 7-19, 21-23 and 28 have been rejected, and claims 24, 25 were objected to.

By this response, please **amend** claims 1, 3, 4, 10-19, 21-23, 25, and **cancel** claims 2, 24.

Rejections

The Examiner rejected claims 1-4, 7,8, 22 and 23 under 35USC103(a) as being anticipated by Ellis (US 2002/0087886) in view of Cloud et al (6,498,739 "Cloud").

Amended claim 1 includes the following features:

> a plurality of shared memory cells, each shared memory cell comprising a magnetic memory cell integrated with a DRAM cell, wherein a word line (WL) is connected to the magnetic memory cell and the DRAM cell;
>
> a plurality of processor elements, each processor element being integrated with a shared memory cell, each processor elements accessing data from a corresponding shared memory cell that is integrated with the processor element, and performing processing on the data.

Support for the amendments can be found throughout the specification, and specifically, in old claim 24. Page 4, last paragraph, states "the non-volatile memory cells 110, 112, 114, 116 can be integrated with the processor elements 120, 122, 124, 126. As will be described, the non-volatile memory cells 110, 112, 114, 116 can be magnetic memory cells. An embodiment includes each magnetic memory cell 110, 112, 114, 116 being formed adjacent to a substrate, and the corresponding processor 120, 122,

124, 126 element being formed in the substrate adjacent to the magnetic memory cell." Page 8, fourth and fifth paragraphs, state " Figure 5 show a circuit schematic of an integrated MRAM cell and DRAM cell according to an embodiment of the invention. The embodiment includes a **shared** DRAM/MRAM cell 500 that includes a first memory cell 510, and a non-volatile memory cell 520 that is interfaced to the first memory cell 510.

The first memory cell 510 can include a DRAM cell. The DRAM cell shown in Figure 5 includes a DRAM controlling transistor QD and a storage capacitor CD. Charge is both stored on the storage capacitor CD, and sensed from the storage capacitor CD through the word line WL and a bit line DBL."

Additionally, support is found on page 7, paragraphs 5 and 6, where it is stated "Figure 3 shows an MRAM cell 200 and processor element 340 according to an embodiment of the invention. The MRAM cell 200 as shown in Figure 3 is formed over a substrate 350. The substrate 350 can include a corresponding processor element 340.

As will be described, the structure shown in Figure 3 is desirable because the MRAM cell 200 does not include any transistor elements. Therefore, the MRAM cell can be formed during the conductor processing of an integrated circuit. That is, semiconductors within the substrate 350 typically include conductive lines formed over the substrate 350. The MRAM cell provides the advantage of being formed during the formation of the conductive lines. This provides ease of producing, and allows the MRAM cell 200 to be formed proximate to the corresponding processor element 340."

Figures 3-9 also provide support for the amended claims. That is, these figures show correspondence/integration between shared memory cells (non-volatile memory cells and DRAM cells) and processor elements.

Claim Rejections Under35USC103(a)

It is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements.

More specifically:

To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP Sec. 2143, *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Paralleling the MPEP references cited above, the Federal Circuit has enunciated several guidelines in making a 35USC103 obviousness determination. A prima facie case of obviousness is established when and only **when the teachings from the prior art itself** would appear to have **suggested** the claimed subject matter to a person of ordinary skill in the art. *In re Bell,* 991 F.2d 783, 26 U.S.P.Q.2d 1529, 1531 (Fed Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051 (C.C.P.A. 1976)). (Emphasis added). "The mere fact that the prior art **may** be modified in the manner suggested by the Examiner does **not** make the modification obvious unless the prior art suggested the desirability of the modification." (Emphasis added) In re Fritch, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

Ellis provides a microchip 90 in which computer component are integrated. Ellis does not describe an interface between DRAM and non-volatile memory. Ellis does not teach integrated magnetic memory cells and DRAM cells in which a word line is connected to a magnetic memory cell and a DRAM cell.

Cloud provides a shadow random access memory cell 800. The shadow RAM cell 800 includes a DRAM cell 801 coupled to a non-volatile memory cell 803. However, Cloud includes **separate** word lines WL1 and WL2 connected to the DRAM cell 801 and the non-volatile memory cell 803.

None of the cited references provide magnetic memory cell integrated with a DRAM cell, wherein a word line (WL) is connected to the magnetic memory cell and the DRAM cell.

Amended claim 1 is patentable over the cited prior art. Claims 3, 4, 7-19, 25, 28 are directly or indirectly dependent on claim 1. Therefore, claims 3, 4, 7-19, 25, 28 are patentable over the prior art.

The Examiner rejected claims 9-21 under 35USC103(a) as being unpatentable over Ellis and Cloud in view of Young (5,621,683).

Claims 9-19, 21, 28 are directly or indirectly dependent on claim 1. Therefore, claims 9-19, 21, 28 are patentable. However, claims 9-19, 21, 28 include additional features that make them further patentable over the cited prior art.

Young teaches a semiconductor memory element comprising a non-volatile memory transistor as a driver transistor and having an adequate difference in output signal from the cell for the different states of the memory transistor to permit the assembly of a large number of such memory cells in an array (column 2, lines 27-36). Reference is made to other thin film circuitry that may perform a logic-function and/or may comprise an active-matrix liquid-crystal display or other flat panel display and/or an image sensor.

Young does not include any suggestions of each processor elements accessing data from a corresponding non-volatile memory cell that is most proximate to the processor element, and performing processing on the data. Young makes no reference of the relative proximity of processor elements and non-volatile memory cells, or the processing of data within non-volatile memory cells. Regarding claim 9, Young makes no suggestions regarding any correspondence between an image sensor and each of the magnetic memory cells. New claim 28 additionally includes the image sensor corresponding with a magnetic memory cell is the image sensor most proximate to the magnetic memory cell.

Claim 13 is additionally patentable over the cited prior art because claim 13 includes the features wherein each image sensor is formed adjacent to a corresponding magnetic memory cell, and each magnetic memory cell is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the magnetic memory cell. Young does not break the image sensors down to a one to one correspondence with magnetic memory cells and processor elements.

Claim 14 is additionally patentable over the cited prior art because claim 14 includes the features wherein each image sensor is formed adjacent to a corresponding magnetic memory cell, and each magnetic memory cell is formed adjacent to a substrate, the substrate comprising a corresponding processor element and DRAM cell formed adjacent to the magnetic memory cell. Young does not break the image sensors down to a one to one correspondence with the non-volatile memory cells, processor elements and DRAM cells. Claim 21 is patentable for similar reasons.

Claim 19 includes the features of a display pixel receives image data from a magnetic memory cell, and wherein the display pixel is an LED and a bias current of the LED is dependent upon a resistance of the magnetic memory cell. Young teaches a very general association between memory and display devices. Young does not provide any correspondence between LEDs and memory elements. Additionally, Young does not provide any teachings of how LEDs are biased based upon connections with the memory, or how the memory accomplishes the biasing.

Independent claims 22, 23 include similar features as claim 1. Therefore, claims 22, 23 are patentable over the prior art.

No new matter has been added by these amendments.

It is believed that all of the pending Claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending Claims (or other Claims) that have not been expressed. Finally nothing in this paper should be construed as an intent to concede any issue with regard to any Claim, except as specifically stated in this paper, and the amendment of any Claim does not necessarily signify concession of unpatentability of the Claim prior to its amendment.

Applicant believes that no fees are currently due; however, should any fee be deemed necessary in connection with this Amendment and Response, the Commissioner is authorized to charge deposit account 08-2025, referencing the Attorney docket number **200207743-1.**

Respectfully submitted,
Manish Sharma

By: Brian Short
Brian Short, Attorney for Applicants
Reg. No. 41,309
Date: Jan 13, 2006
Ph. No.: 408-888-9830